CLC014 Adaptive Cable Equalizer for High-Speed Data Recovery

Check for Samples: CLC014

FEATURES

- **Automatic Equalization of Coaxial and Twisted Pair Cables**
- **Carrier Detection and Output Mute**
- **Output Eye Monitor**
- **Single Supply Operation: +5V or −5.2V**
- **Single-Ended or Differential Input**
- **Low Cost**

APPLICATIONS

- **SMPTE 259M Serial Digital Interfaces: NTSC/PAL, 4:2:2 Component and Wide Screen; also 540 Mbps (4:4:4:4)**
- **Serial Digital Video Routing and Distribution**
- **Serial digital Data Equalization and Reception**
- **Data Recovery Equalization: ATM, CAD Networks, Medical, Set Top Terminals, industrial Video Networks**

KEY SPECIFICATIONS

- **Low Jitter: 180ps$_{pp}$ @ 270 Mbps through 200 Meters of Belden 8281 Coaxial Cable**
- **High Data Rates: < 50 Mbps to > 650 Mbps**
- **Excellent Input Return Loss: 19 dB @ 270 MHz**
- **Low Supply Current: 58 mA**
- **Equalizes up to 300+ Meters of Belden 8281 or 120 Meters of Cat 5 UTP Cable**

DESCRIPTION

Texas Instruments' CLC014 adaptive cable equalizer is a low-cost monolithic solution for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The CLC014 simplifies the task of high-speed data recovery with a one-chip solution and a minimal number of external components. The equalizer automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 40 dB at 200 MHz. This corresponds to 300 meters of Belden 8281 or 120 meters of Category 5 UTP (unshielded twisted pair).

The CLC014 provides superior jitter performance: 180ps$_{pp}$ for 270 Mbps data that has passed through 200 meters of Belden 8281 cable. This exceptional performance provides wide error margin in digital data links. The equalizer operates on a single supply with a power consumption of only 290 mW. The small 14-pin SOIC package allows for high-density placement of components for multi-channel applications such as routers. The equalizer operates over a wide range of data rates from less than 50 Mbps to rates in excess of 650 Mbps.

The equalizer is flexible in allowing either single-ended or differential input drive. Its high common mode rejection provides excellent immunity to interference from noise sources. On-chip quantized feedback eliminates baseline wander.

Additional features include a carrier detect output and an output mute pin which, when tied together, mute the output when no signal is present. A buffered eye monitor output is provided, for viewing the equalized signal prior to the comparator. Differential AEC pins allow the user to set the internal adaptive loop time constant with one external capacitor. Also, the CLC014 is insensitive to the pathological patterns inherent in the video industry standards.

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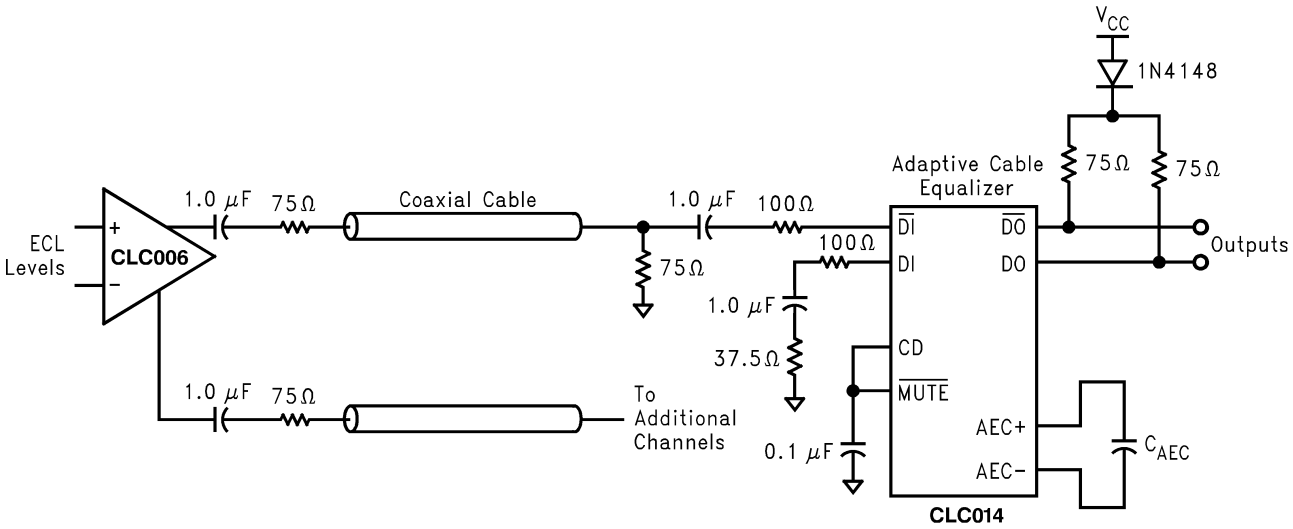
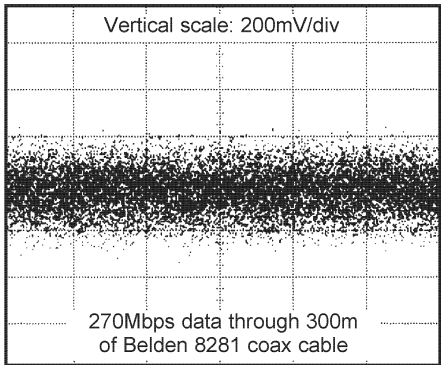
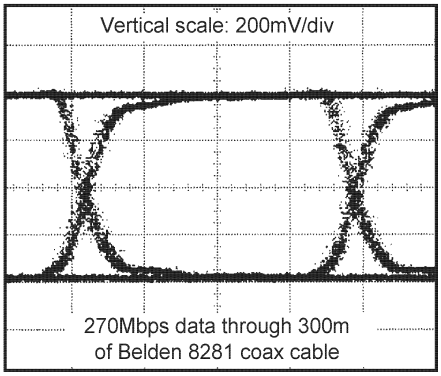
TYPICAL APPLICATION



Before Equalization



After Equalization



Connection Diagram

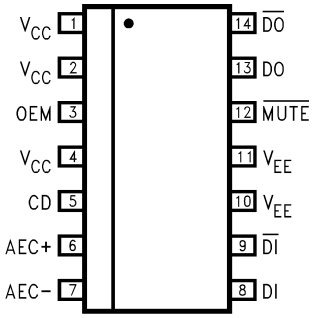


Figure 1. 14-Pin SOIC (Top View)
See D Package

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (V_{CC}–V_{EE})		−0.3V, +6.5V
Maximum Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature	(Soldering 4 sec.)	+260°C
ESD Rating (3)		<500V
θ_{JA} 14-Pin SOIC (D)		95°C/W
MTTF (based on limited life test data)		4.8 x 10^7 hours

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5 kΩ in series with 100 pF; based on limited test data.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC}–V_{EE})	4.5V to 5.5V
Operating Temperature Range	−40°C to +85°C
Series Input Resistance (In Series w/DI & $\overline{DI}$)	100Ω
Input Coupling Capacitance	1.0 µF
AEC Capacitor (Connected between AEC+ & AEC−)	50 pF to 1 µF
Cable Input Voltage Swing (1)	720 to 880 mV_{pp}
DO/$\overline{DO}$ Minimum Voltage (2)	V_{CC}–1.6V

(1) These specifications assume an 800 mV_{pp} signal at the cable input. Levels above and below 800 mV are allowable, but performance may vary. The cable will attenuate the signal prior to entering the equalizer.
(2) To maintain specified performance, do not reduce DO/$\overline{DO}$ below this level.

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ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, signal source swing = 0.8 V_{pp} (1), C_{AEC} = 100 pF)

Parameter	Conditions	Typ +25°C	Min/Max +25°C	Min/Max −40°C to +85°C	Units
DYNAMIC PERFORMANCE					
Residual Jitter					
100 meters Belden 8281	270 Mbps PRN (2)	150	250	400	ps_{pp}
200 meters Belden 8281	270 Mbps PRN (2)	180	250	400	ps_{pp}
300 meters Belden 8281	270 Mbps PRN (3)(2)	350	500	750	ps_{pp}
Equalization Time Constant					
100 meters Belden 8281	C_{AEC} = 100 pF (4)	1.5	_	_	µs
200 meters Belden 8281	C_{AEC} = 100 pF (4)	2.0	_	_	µs
300 meters Belden 8281	C_{AEC} = 100 pF (4)	3.2	_	_	µs
output rise and fall time (20%–80%)	$R_{collector}$ = 75Ω	750	_	_	ps
output duty cycle distortion		30	_	_	ps
minimum average transition density		1/50	_	_	trans/ns
maximum average data rate	150m Belden 8281 (5)	650	_	_	Mbps
V_{CC} Jitter Sensitivity					
27 MHz		0.85	_	_	ns/V
270 MHz		1.90	_	_	ns/V
V_{EE} Jitter Sensitivity					
27 MHz		0.55	_	_	ns/V
270 MHz		1.45	_	_	ns/V
STATIC PERFORMANCE					
Supply Current (Includes Output Current)					
V_{AEC} = 0V	(3)	58	48/68	40/75	mA
V_{AEC} = 0.4V	(3)	53	43/64	37/70	mA
Input and Output Parameters					
DO/$\overline{DO}$ output current		10	8.7/11.3	8.0/12	mA
DO/$\overline{DO}$ output voltage swing	$R_{collector}$ = 75Ω (3)	750	650/850	600/900	mV
DI/$\overline{DI}$ common mode voltage		3.4	_	_	V
AEC differential voltage	Belden 8281	1.5	_	_	mV/meter
AEC+/AEC− common mode		3.6	_	_	V
output eye monitor (OEM) bias potential		3.2	_	_	V
carrier detect (CD) current output-HIGH	CD V_{OH} = 4.5V	−400	_	_	µA
carrier detect (CD) current output-LOW	CD V_{OL} = 0.5V	600	_	_	µA
$\overline{MUTE}$ voltage input-HIGH	(3)	1.8	2.0	2.0	V
$\overline{MUTE}$ voltage input-LOW	(3)	1.2	0.8	0.8	V
$\overline{MUTE}$ current input-HIGH	V_{IH} = 5V (3)	5.0	±100	±500	nA
$\overline{MUTE}$ current input-LOW	V_{IL} = 0V (3)	0.2	±100	±500	nA

(1) These specifications assume an 800 mV_{pp} signal at the cable input. Levels above and below 800 mV are allowable, but performance may vary. The cable will attenuate the signal prior to entering the equalizer.
(2) Peak-to-peak jitter is defined as 6 times the rms jitter.
(3) J-level: spec. is 100% tested at +25°C.
(4) For more information, see OPERATION and Design Guidelines.
(5) 50% eye opening.

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = 0V, signal source swing = 0.8 V_{pp} (1), C_{AEC} = 100 pF)

Parameter	Conditions	Typ +25°C	Min/Max +25°C	Min/Max −40°C to +85°C	Units
TIMING PERFORMANCE					
CD Response Time					
carrier applied	(6)	1.0	_	_	µs
carrier removed	(7)	12	_	_	µs
$\overline{\text{MUTE}}$ response time	(8)	2.0	_	_	ns
MISCELLANEOUS PERFORMANCE					
input resistance	single-ended	7.3	_	_	kΩ
input capacitance	single-ended (9)	1.0	_	_	pF
input return loss @ 270 MHz	Z_o = 75Ω (10)	19	_	_	dB
maximum cable attenuation	200 MHz (11)	40	_	_	dB

(6) Time from application of a valid signal to when the CD output asserts high.
(7) Time from the removal of a valid signal to when the CD output asserts low.
(8) Time from assertion of $\overline{\text{MUTE}}$ to when the output responds.
(9) Device only. Does not include typical pc board parasitics.
(10) Includes typical pc board parasitics.
(11) This sets the maximum cable length for the equalizer.

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TYPICAL PERFORMANCE CHARACTERISTICS

Before Equalization:
100m of Belden 8281 Coaxial Cable

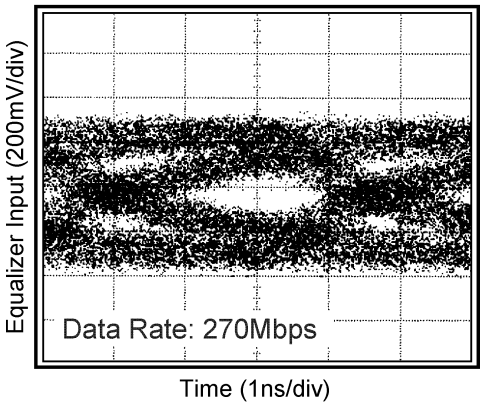

Figure 2.

After Equalization:
100m of Belden 8281 Coaxial Cable

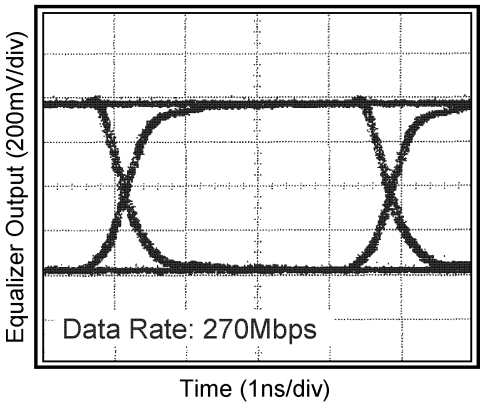

Figure 3.

Before Equalization:
200m of Belden 8281 Coaxial Cable

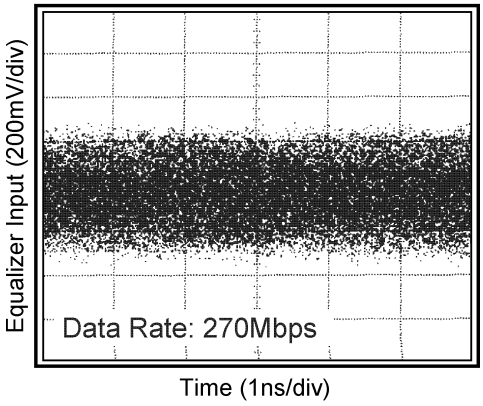

Figure 4.

After Equalization:
200m of Belden 8281 Coaxial Cable

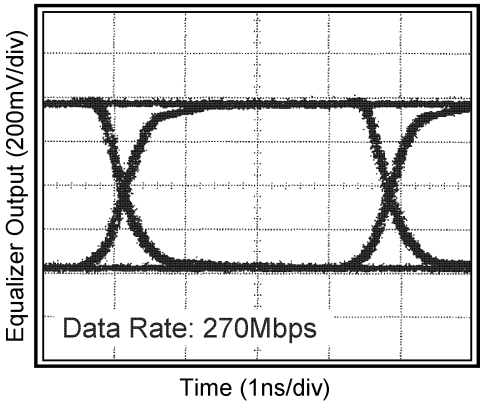

Figure 5.

Before Equalization:
300m of Belden 8281 Coaxial Cable

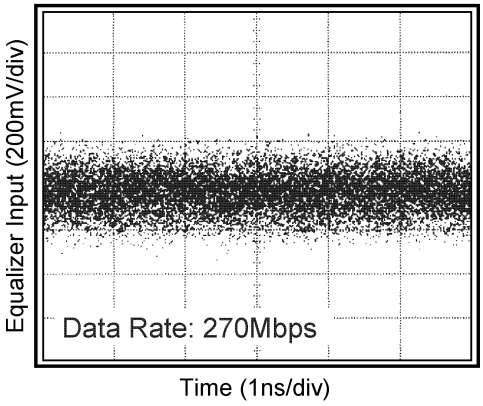

Figure 6.

After Equalization:
300m of Belden 8281 Coaxial Cable

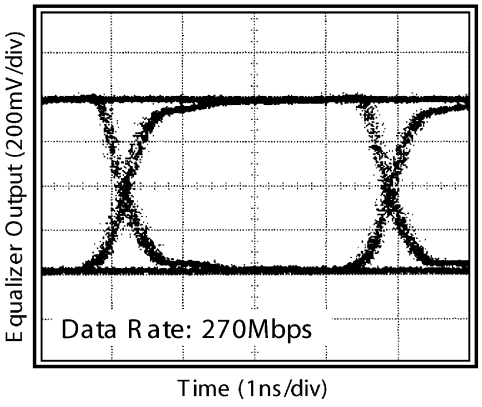

Figure 7.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Before Equalization:
100m Category 5 UTP at 51.7Mbps

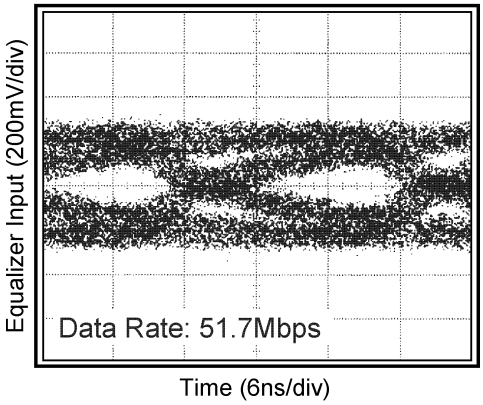

Figure 8.

After Equalization:
100m Category 5 UTP at 51.7Mbps

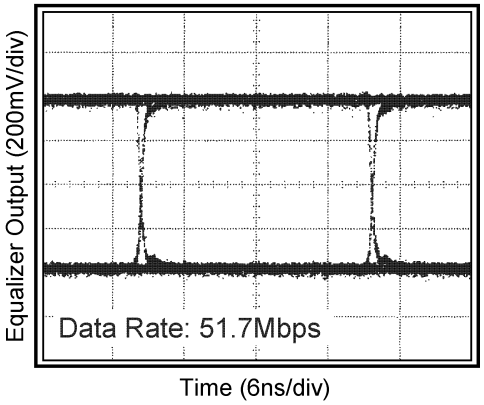

Figure 9.

Before Equalization:
100m Category 5 UTP at 155Mbps

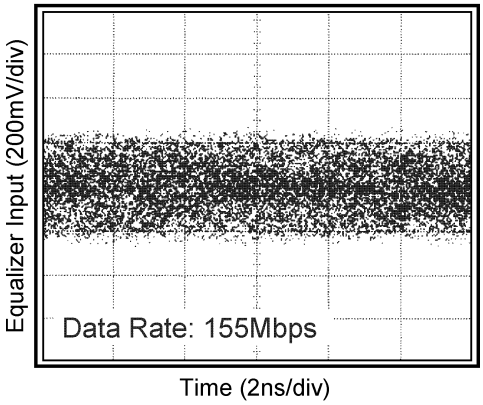

Figure 10.

After Equalization:
100m Category 5 UTP at 155Mbps

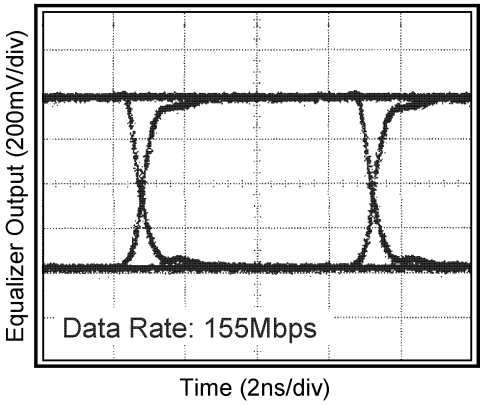

Figure 11.

Before Equalization:
100m Category 5 UTP at 311Mbps

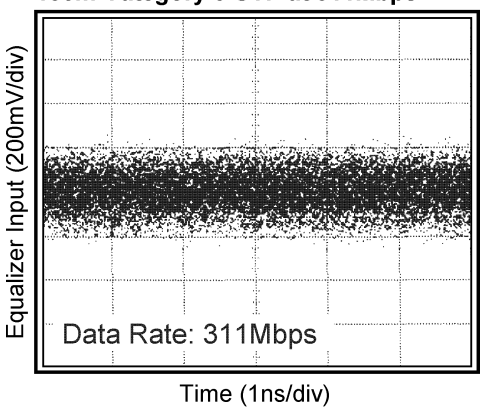

Figure 12.

After Equalization:
100m Category 5 UTP at 311Mbps

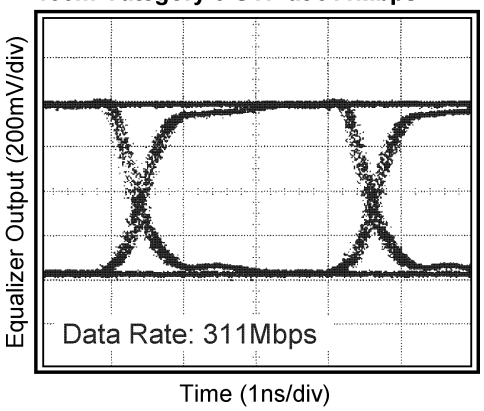

Figure 13.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

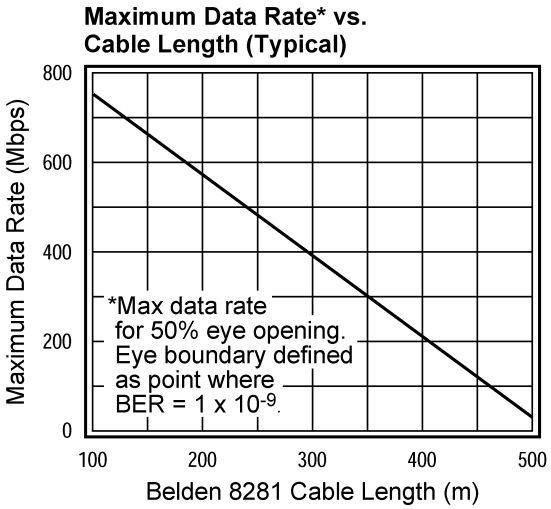

Figure 14.

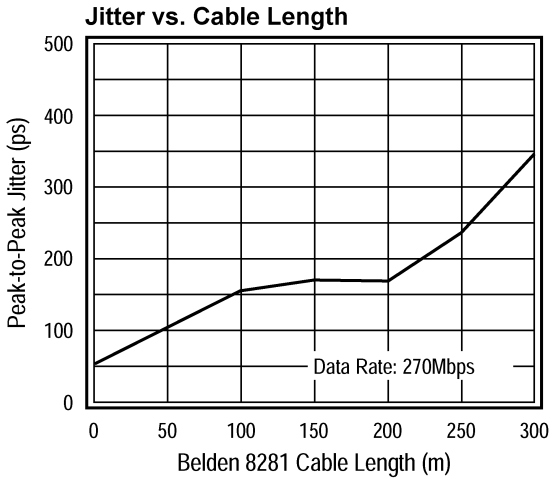

Figure 15.

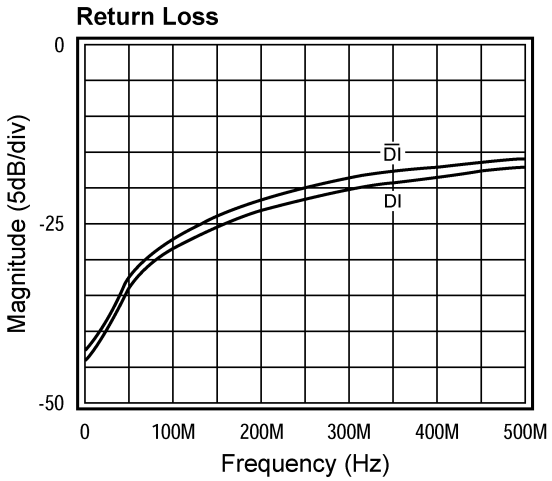

Figure 16.

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PIN DEFINITIONS

Name	Pin #	Description
DI, $\overline{DI}$	8, 9	Differential data inputs.
DO, $\overline{DO}$	13, 14	Differential collector data outputs (ECL compatible).
AEC+, AEC−	6, 7	AEC loop filter pins. A capacitor connected between these pins governs the loop response for the adaptive equalization loop.
OEM	3	Eye monitor output. The output of the equalization filter.
CD	5	Carrier detect. (Low when no signal is present).
$\overline{MUTE}$	12	Output $\overline{MUTE}$. (Active low.) Carrier detect may be tied to this pin to inhibit the output when no signal is present.
V_{CC}	1, 2, 4	Positive supply pins (ground or +5V).
V_{EE}	10, 11	Negative supply pins (−5.2V or ground).

OPERATION

The CLC014 Adaptive Cable Equalizer provides a complete solution for equalizing high-bit-rate digital data transmitted over long transmission lines. The following sections furnish design and application information to assist in completing a successful design:

- Block diagram explanation of the CLC014
- Recommended standard input and output interface connections
- Common applications for the CLC014
- Measurement, PC layout, and cable emulation boxes

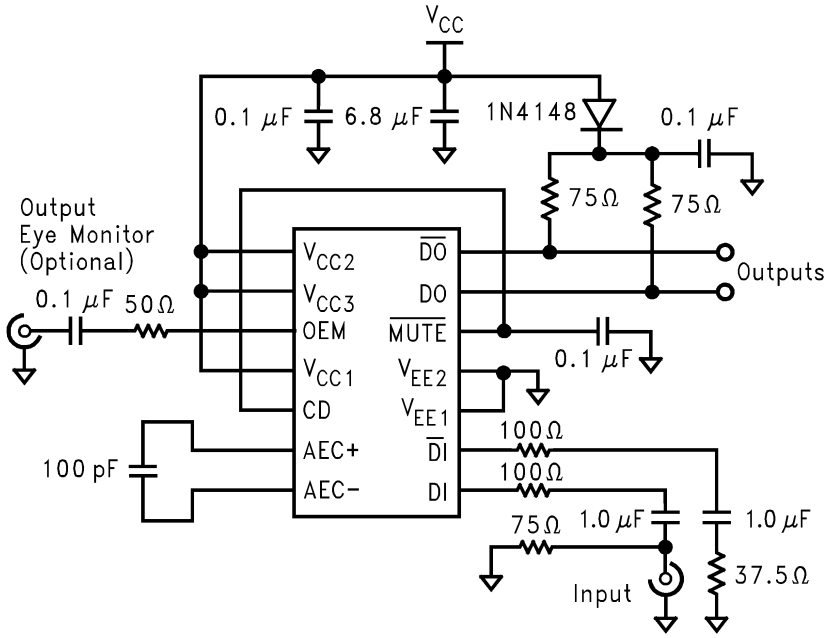

Figure 17. CLC014 Equalizer Application Circuit

BLOCK DESCRIPTION

The CLC014 is an adaptive equalizer that reconstructs serial digital data received from transmission lines such as coaxial cable or twisted pair. Its transfer function approximates the reciprocal of the cable loss characteristic. The block diagram in Figure 18 depicts the main signal conditioning blocks for equalizing digital data at the receiving end of a cable. The CLC014 receives baseband differential or single-ended digital signals at its inputs DI and $\overline{DI}$.

The ***Equalizer*** block is a two-stage adaptive filter. This filter is capable of equalizing cable lengths from zero meters to lengths that require 40 dB of boost at 200 MHz.

The ***Quantized Feedback Comparator*** block receives the differential signals from the equalizer filter block. This block includes two comparators. The first comparator incorporates a self-biasing DC restore circuit. This is followed by a second high-speed comparator with output mute capability. The second comparator receives and slices the DC-restored data. Its outputs DO and $\overline{DO}$ are taken from the collectors of the output transistors. $\overline{MUTE}$ latches DO and $\overline{DO}$ when a TTL logic low level is applied.

The ***Adaptive Servo Control*** block produces the signal for controlling the filter block, and outputs a voltage proportional to cable length. It receives differential signals from the output of the filter block and from the quantized-feedback comparator (QFBC) to develop the control signal. The servo loop response is controlled by an external capacitor placed across the AEC+ and AEC− pins. Its output voltage, as measured differentially across AEC+ and AEC−, is roughly proportional to the length of the transmission line. For Belden 8281 coaxial cable this differential voltage is about 1.5 mV/meter. Once this voltage exceeds 500 mV, no additional equalization is provided.

The ***Carrier Detect (CD)*** block monitors the signal power out of the equalizing filter and compares it to an internal reference to determine if a valid signal is present. A CMOS high output indicates that data is present. The output of CD can be connected to the $\overline{MUTE}$ input to automatically latch the outputs (DO and $\overline{DO}$), preventing random transitions when no data is present.

The ***Output Eye Monitor (OEM)*** provides a single-ended buffered output for observing the equalized eye pattern. The OEM output is a low impedance high-speed voltage driver capable of driving an AC-coupled 100Ω load.

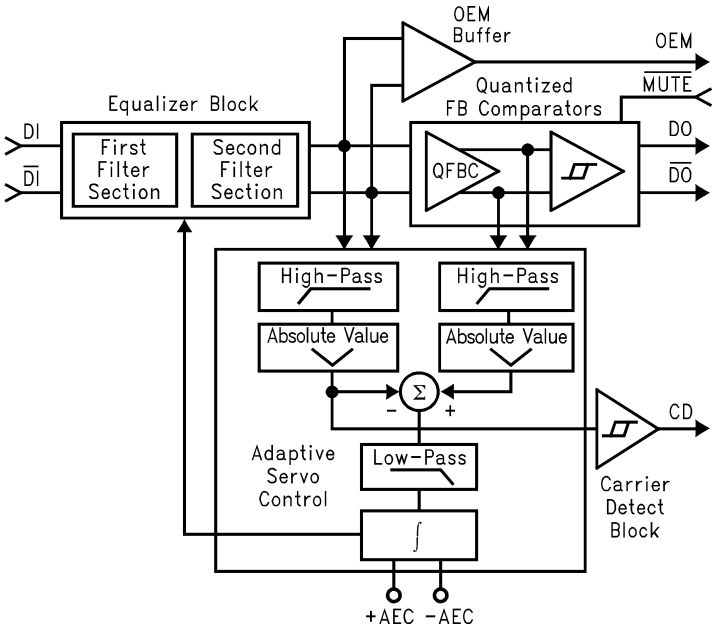

Figure 18. CLC014 Block Diagram

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DEVICE TESTING

Performance or compliancy testing of the CLC014 with **Cable Clones** is not allowed. Use of these devices is contrary to the product's specifications and test procedures. Testing for product specifications or performance using cable clones is invalid since cable clones have a different frequency response than the actual cable. Testing with full length cable samples is recommended.

Input Interfacing

The CLC014 accepts either differential or single-ended input voltage specified in Static Performance. The following sections show several suggestions for interfaces for the inputs and outputs of the CLC014.

SINGLE-ENDED INPUT INTERFACE: 75Ω Coaxial Cable

The input is connected single-ended to either DI or $\overline{DI}$ as shown in Figure 19. Balancing unused inputs helps to lessen the effects of noise. Use the equivalent termination of 37.5Ω to balance the input impedance seen by each pin. It also helps to terminate grounds at a common point. Resistors R_x and R_y are recommended for optimum performance. The equalizer inputs are self-biasing. Signals should be AC coupled to the inputs as shown in Figure 19.

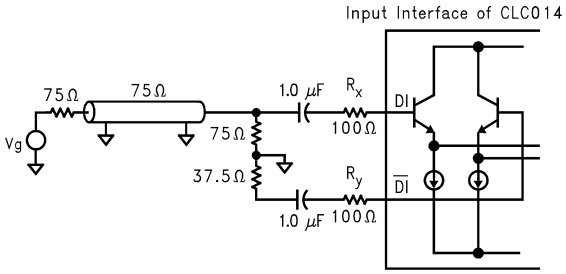

Figure 19. Single-Ended 75Ω Cable Input Interface

DIFFERENTIAL INPUT INTERFACE: Twisted Pair

A recommended differential input interface is shown in Figure 20. Proper voltage levels must be furnished to the input pins and the proper cable terminating impedance must be provided. For Category 5 UTP this is approximately 100Ω. Figure 20 shows a generalized network which may be used to receive data over a twisted pair. Resistors R_1 and R_2 provide the proper terminating impedance and signal level adjustment. The blocking capacitors provide AC coupling of the attenuated signal levels. The plots in TYPICAL PERFORMANCE CHARACTERISTICS demonstrate various equalized data rates using Category 5 UTP at 100 meter lengths. A full schematic of a recommended driver and receiver circuit for 100Ω Category 5 UTP is provided in Typical Applications.

$$R_1 = \frac{Z_o}{V_{pp}}\left(\frac{V_{pp}-1.6}{2}\right) \qquad R_2 = \frac{0.8Z_o}{V_{pp}} \tag{1}$$

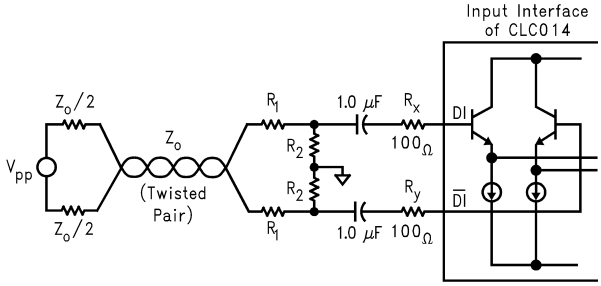

Figure 20. Twisted Pair Input Interface

Output Interfacing

The outputs DO and $\overline{DO}$ produce ECL logic levels when the recommended output termination networks are used. The DO and $\overline{DO}$ pins are ***not complementary emitter coupled logic*** outputs. Instead, the outputs are taken off of the collectors of the transistors. Therefore, care must be taken to meet the interface threshold levels required by ECL families. Recommended interfaces for standard ECL families are shown in the following circuits.

DIFFERENTIAL LOAD-TERMINATED OUTPUT INTERFACE

Figure 21 shows a recommended circuit for implementing a differential output that is terminated at the load. A diode or 75Ω resistor provides a voltage drop from the positive supply (+5V for PECL or Ground for ECL operation) to establish proper ECL levels. The resistors terminate the cable to the characteristic impedance. The output voltage swing is determined by the CLC014 output current (10 mA) times the termination resistor. For the circuit in Figure 21, the nominal output voltage swing is 750 mV.

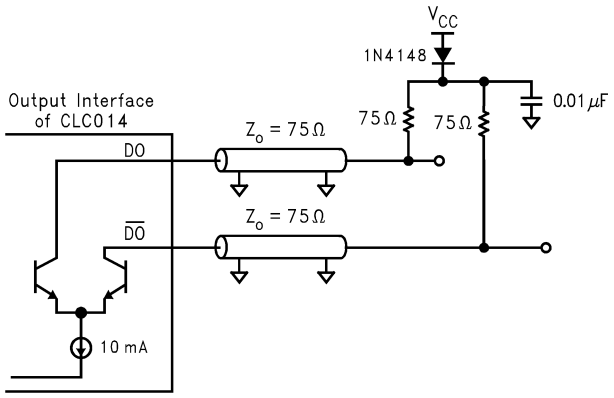

Figure 21. Differential Load Terminated Output Interface

DIFFERENTIAL SOURCE-TERMINATED OUTPUT INTERFACE

Figure 22 is similar to Figure 21 except that the termination is provided at the source. This configuration may also be used for single-ended applications. However, the unused output must still be terminated as shown.

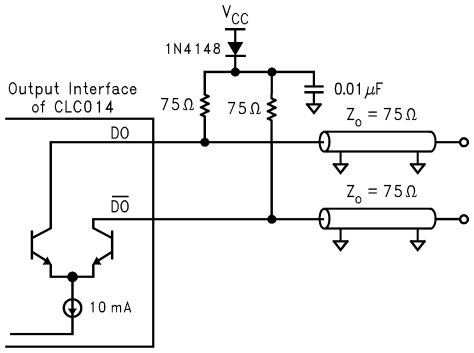

Figure 22. Differential Source Terminated Output Interface

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TERMINATING PHYSICALLY SEPARATED OUTPUTS

When the two outputs must be routed to physically separate locations, the circuit in Figure 22 may be applied. Alternatively, if load termination is desired, the circuit in Figure 23 may be used. The resistive divider network provides 75Ω termination and establishes proper ECL levels. This circuit consumes slightly more power than the previous circuits.

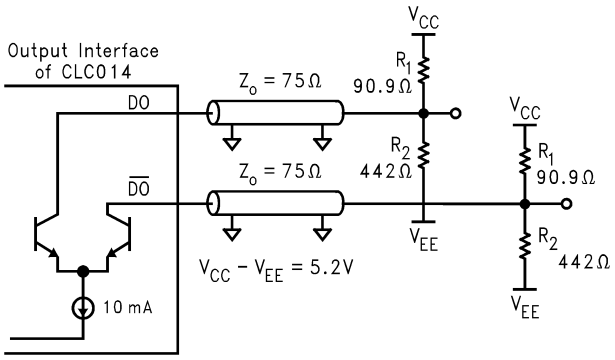

Figure 23. Alternative Load Terminated Output Interface

Design Guidelines

SELECTING THE AUTOMATIC EQUALIZER CAPACITOR

The AEC capacitor sets the loop time constant τ for the equalizer's adaptive loop response time. The following formula is used to set the loop time constant:

$$\tau = R \bullet C_{AEC} \bullet 10^{-6} \quad (2)$$

R is a conversion factor that is set by internal equalizer parameters and cable length. For Belden 8281 coaxial cable, the R values are (τ = μs, C_{AEC} in pF):

Cable Length	R Value (Ohms)
100 meters	15000
200 meters	20000
300 meters	32000

For example, a C_{AEC} value of 100 pF results in an adaptive loop time constant of 2 μs at 200 meters of cable.

CONNECTION AND OPERATION OF CD AND $\overline{MUTE}$

Carrier Detect (CD) is a CMOS output that indicates the presence of equalized data from the filter. This CD output can be connected to $\overline{MUTE}$ to suspend changes in the data outputs DO and $\overline{DO}$, if no valid signal exists. This simple configuration prevents random output transitions due to noise. For sparse transition patterns it is recommended that a capacitor be connected to CD as shown in Figure 17.

Add a capacitor to pin 5 to slow the response time of Carrier Detect when Carrier Detect is connected to $\overline{MUTE}$. The capacitor reduces sensitivity to pathological patterns. Pathological patterns are defined as sparse data sequences with few transitions.

OUTPUT EYE MONITOR OEM CONNECTIONS

The OEM is a high-speed, buffered output for monitoring the equalized eye pattern prior to the output comparator. Its output is designed to drive an AC-coupled 50Ω coaxial cable with a series 50Ω backmatch resistor. The cable should be terminated with 50Ω at the oscilloscope. Figure 17 shows a schematic with a typical connection.

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MINIMUM DATA TRANSITIONS

The CLC014 specifies a minimum transition rate. For the CLC014 this sets the minimum data rate for transmitting data through any cable medium. The CLC014 minimum average transition density is found in the ELECTRICAL CHARACTERISTICS.

POWER SUPPLY OPERATION AND THERMAL CONSIDERATIONS

The CLC014 operates from either +5V or −5.2V single supplies. Refer to Figure 17 when operating the part from +5V. When operating with a −5.2V supply, the V_{EE} pins should be bypassed to ground. The evaluation board and associated literature provide for operation from either supply.

Maximum power dissipation occurs at minimum cable length. Under that condition, I_{CC} = 58 mA.

Total power dissipated:

$$P_T = (58\text{ mA})(5\text{V}) = 290\text{ mW} \quad (3)$$

Power in the load:

$$P_L = (0.7\text{V})(11\text{ mA}) + (37.5)(11\text{ mA})^2 = 12\text{ mW} \quad (4)$$

Maximum power dissipated on the die:

$$P_{DMAX} = P_T – P_L = 278\text{ mW} \quad (5)$$

Junction Temperature =

$$(\theta_{JA})(278\text{ mW}) + T_A = T_A + 26°\text{C} \quad (6)$$

Layout and Measurement

The printed circuit board layout for the CLC014 requires proper high-speed layout to achieve the performance specifications found in the datasheet. The following list contains a few rules to follow:

1. Use a ground plane.
2. Decouple power pins with 0.1 µF capacitors placed ≤ 0.1” (3mm) from the power pins.
3. Design transmission strip lines from the CLC014's input and output pins to the board connectors.
4. Route outputs away from inputs.
5. Keep ground plane ≥ 0.025” (0.06mm) away from the input and output pads.

Figure 24 shows a block level measurement diagram, while Figure 31 on depicts a detailed schematic. A pseudo-random pattern generator with low output jitter was used to provide a NRZI pattern to create the eye diagrams shown in TYPICAL PERFORMANCE CHARACTERISTICS.

Since most pattern generators have a 50Ω output impedance, a translation can be accomplished using a CLC006 Cable Driver as an impedance transformer. A wide bandwidth oscilloscope is needed to observe the high data rate eye pattern. When monitoring a single output that is terminated at both the equalizer output and the oscilloscope, the effective output load is 37.5Ω. Consequently, the signal swing is half that observed for a single-ended 75Ω termination.

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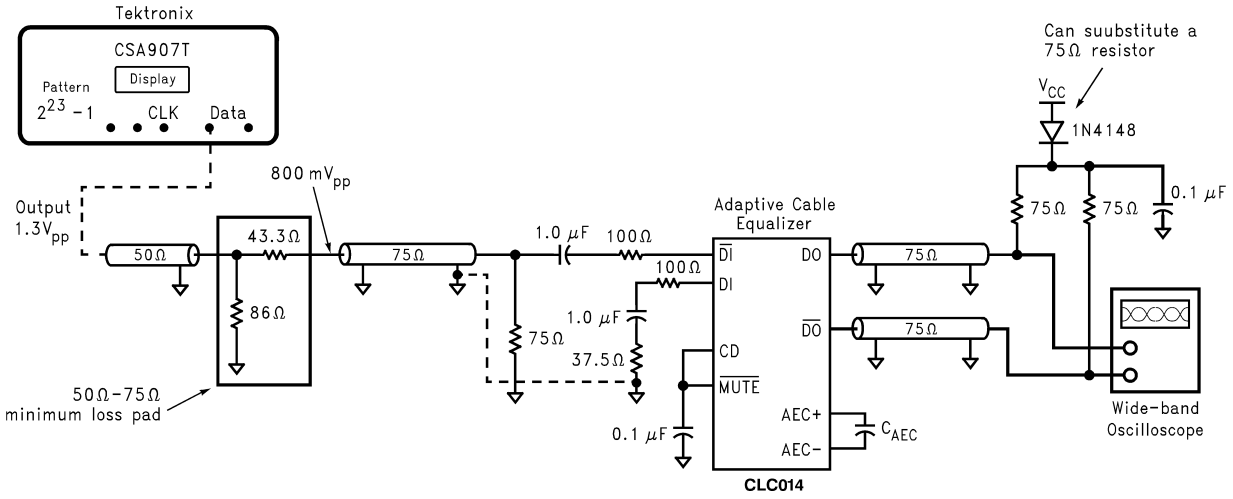

Figure 24. Typical Measurement Block

Troubleshooting with scope probes can affect the equalization. For high data rates, use a ***low capacitance probe*** with less than 2 pF probe capacitance. Evaluation boards and literature are available for quick prototyping and evaluation of the CLC014 Adaptive Cable Equalizer. The CLC014 contains CMOS devices and operators should ***use grounding straps when handling*** the parts.

Figure 25 shows the CLC014's internal power supply routing. Bypass V_{CC} (pin 4) by:

- Monolithic capacitor of about 0.1 µF placed less than 0.1" (3mm) from the pin
- Tantalum capacitor of about 6.8 µF for large current signal swings placed as close as convenient to the CLC014

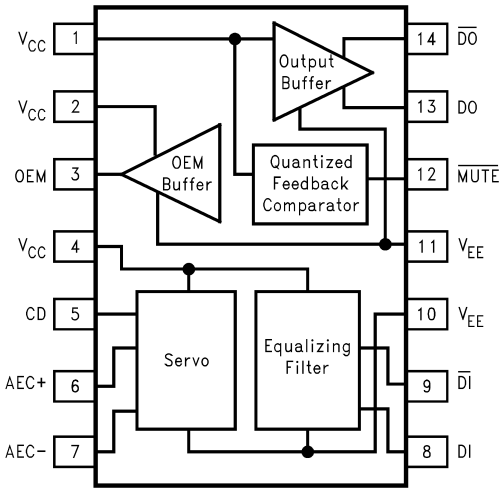

Figure 25. Power Package Routing Fixture

To minimize ringing at the CLC014's inputs, place a 100Ω resistor in series with the input. This resistor reduces inductance effects.

Several layout techniques can improve high speed performance:

- Keep input, output and AEC traces well separated
- Use balanced input termination's
- Avoid routing traces close to the CLC014's input trace
- Maintain common return points for components
- Use guard traces

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The input lines of the CLC014 use a 100Ω series resistors at the input pins. This decreases the inductive effects internal to the part to reduce ringing on fast rise and fall times. Refer to the evaluation board layout for further suggestions on layout for the CLC014 Adaptive Equalizer.

EQUALIZATION CURVE

The CLC014 Adaptive Cable Equalizer has a maximum equalization response as shown in Figure 26. This response may be obtained by forcing >0.5V differentially at the AEC pins.

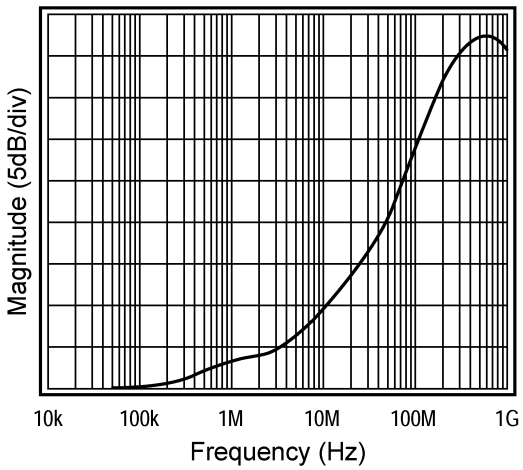

Figure 26. Maximum Equalization Response

CABLE EMULATION BOXES

Some cable emulation boxes will not mimic cables correctly. When evaluating the CLC014, it is strongly recommended that actual cable be used to determine the various performance parameters.

Typical Applications

COAXIAL CABLE RECEIVER (Page 1)

The CLC014 equalizer application shown on page 1 will equalize a variety of coaxial cables up to lengths that attenuate the signal by 40 dB at 200 MHz. The application shows the proper connection for a single cable driven with a CLC006 driver. Carrier Detect (CD) is connected to $\overline{\text{MUTE}}$ to latch outputs DO and $\overline{\text{DO}}$ in the absence of an input signal to the equalizer.

Refer to the CLC014's evaluation board layout for additional suggestions.

Texas Instruments can supply most of the major components required to design a transmission line repeater. Figure 27 shows a typical repeater design using the CLC006, CLC014, and the CLC016. The design functions supported by each chip are:

CLC006: Cable connection chip
Boosts drive for transmission to next repeater or final destinations

CLC014: Receive serialized digital data from incoming transmission lines
Equalizes the incoming data

CLC016: Retimes the equalized data (improving jitter)

The CLC016 is a multi-rate data retiming PLL. The circuit (Figure 27) will work at up to 4 different data rates with no additional components or manual tuning.

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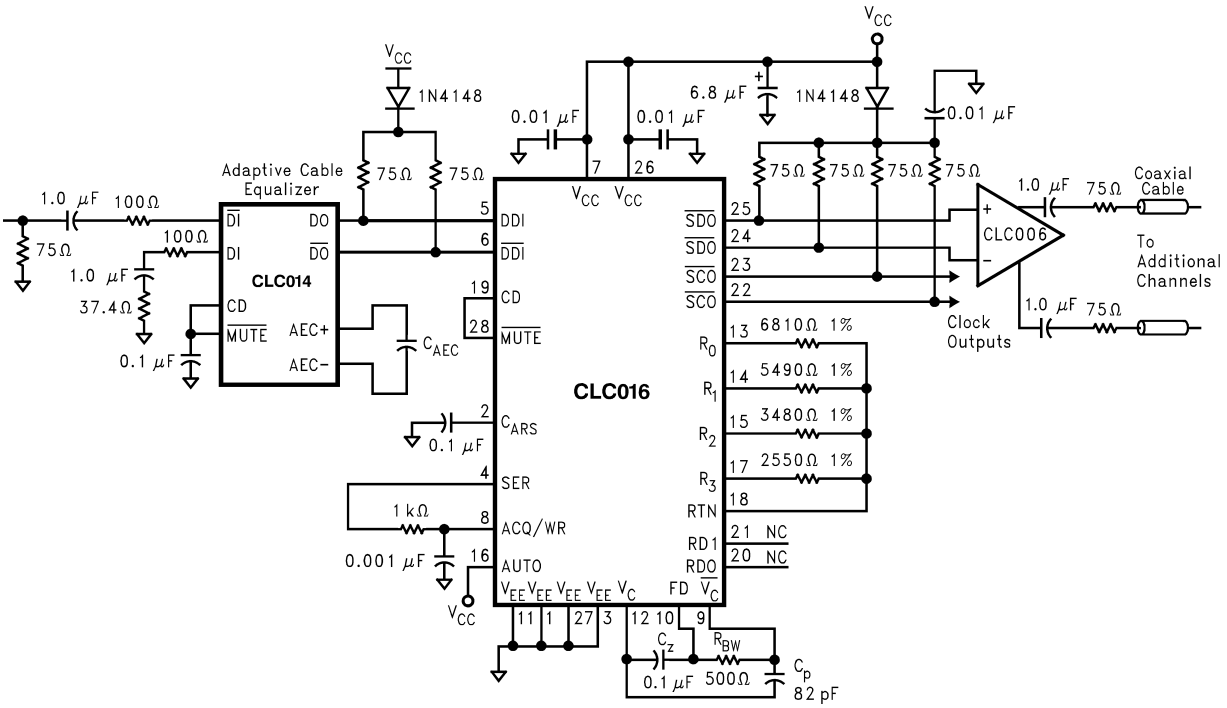

Figure 27. Typical Repeater Design

DIGITAL VIDEO (SDV) ROUTERS

The CLC014 provides performance that complies with the SMPTE 259M standard for serial digital video (SDV) transmission over coaxial cable. One common application is in SDV routers, which provide a switching matrix for connecting video source equipment (e.g., cameras) to destination equipment (e.g., video tape recorders, monitors, etc.).

Figure 28 shows a typical configuration for an SDV router, including equalizers, a crosspoint switch, data retimers, and cable drivers. The CLC014 is used in its standard configuration in this application, and automatically equalizes cable lengths from zero meters to greater than 300 meters at 360 MHz (see plots in TYPICAL PERFORMANCE CHARACTERISTICS). The equalized outputs are connected to the differential inputs of the crosspoint switch. The CLC016 Data Retimer receives the data from the crosspoint and performs the clock and data recovery functions, further reducing jitter. Finally, the retimed data is driven into the coaxial cable by a CLC006 Cable Driver (with two amplitude-adjustable outputs) or a CLC007 Cable Driver (with four outputs).

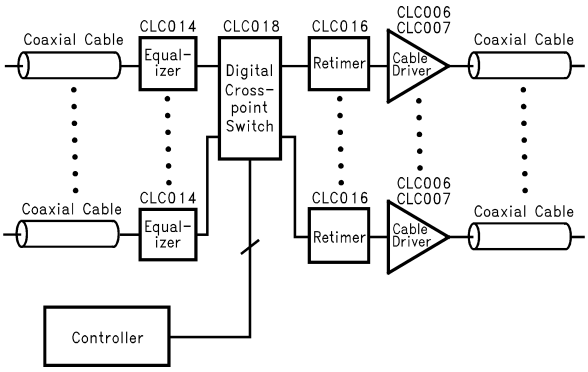

Figure 28. Video Routing Block Diagram

TWISTED PAIR DRIVER

A low-cost medium for transmitting data is twisted pair. Category 5 UTP has an attenuation characteristic similar to Belden 8281 coaxial cable but scaled in length: 120 meters of Category 5 UTP is roughly equivalent to 300 meters of Belden 8281 cable. When properly implemented, the CLC014 will equalize data rates up to 625 Mbps over Category 5 UTP. The maximum data rate depends upon the cable length. A plot of Maximum Data Rate vs Cable Length is found in TYPICAL PERFORMANCE CHARACTERISTICS for Belden 8281, and can be scaled as stated above to estimate maximum cable lengths and data rates for UTP.

Category 5 UTP has a characteristic impedance of approximately 100Ω. The CLC006 in Figure 29 is used to drive the twisted pair AC-coupled with a series 0.1 µF capacitor and a 50Ω resistor in each differential output. The CLC014 Adaptive Equalizer requires 800 mV_{pp} from the transmit side of the cable. A voltage divider is necessary to scale the voltage to the required level at the input of the CLC014. This resistor network also provides the correct impedance match for twisted pair.

For Category 5 UTP, the approximate AEC voltage per length is 3.75 mV/m (see BLOCK DESCRIPTION). The CLC006 provides a trim adjust for fine tuning the output signal with the resistor R. Refer to the CLC006/007 datasheet for tuning directions.

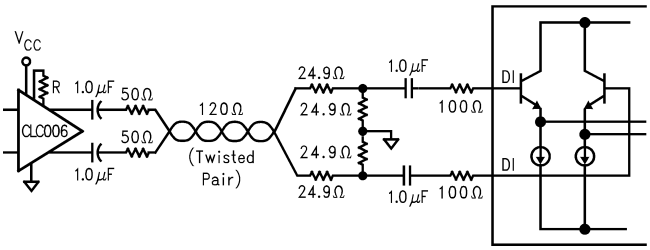

Figure 29. Twisted Pair Equalization

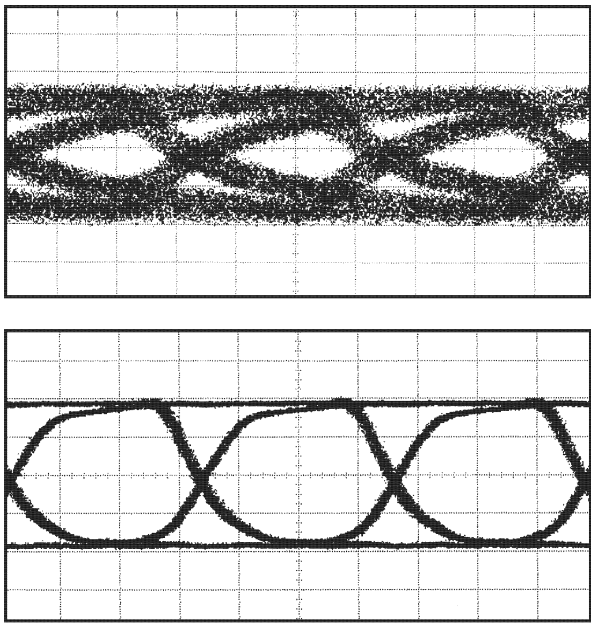

Figure 30. Before and After Equalization at 622 Mbps Through 50 Meters of Category 5 UTP

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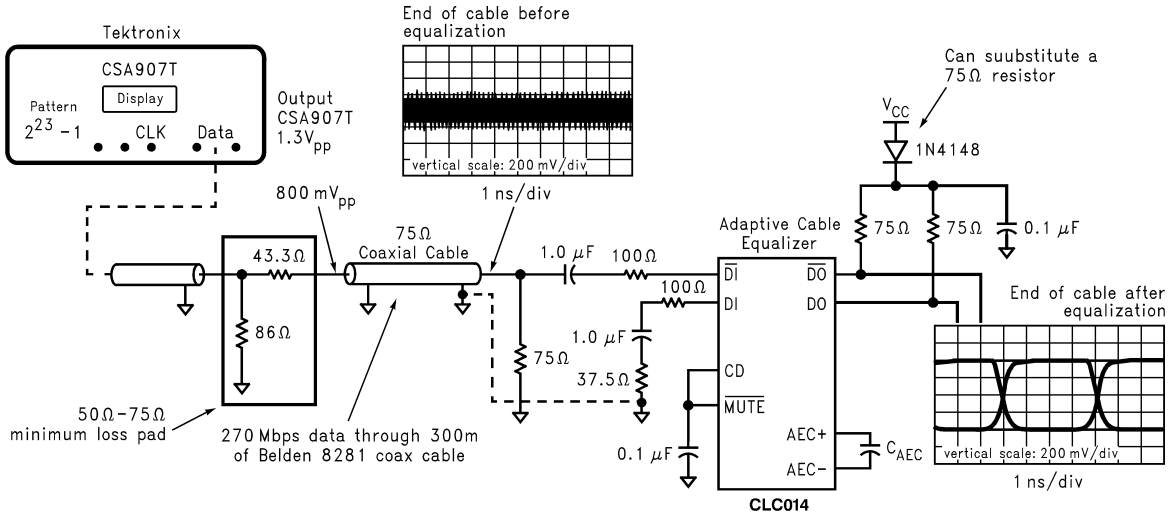

Figure 31. Typical Measurement Setup

Evaluation Board

Evaluation boards are available for a nominal charge that demonstrate the basic operation of the SDI/SDV/SDH devices. The evaluation boards can be ordered through Texas Instruments' Distributors. Supplies are limited, please check for current availability.

The SD014EVK evaluation kit for the CLC014, Adaptive Cable Equalizer for High-Speed Data Recovery, provides an operating environment in which the cable equalizer can be evaluated by system / hardware designers. The evaluation board has all the needed circuitry and connectors for easy connection and checkout of the device circuit options as discussed in the CLC014 datasheet. A schematic, parts list and pictorial drawing are provided with the board.

- Device Datasheet and / or EVK User Manual
- View a picture of the EVK
- View the EVK Schematic
- View the top assembly drawing and BOM
- View the bottom assembly drawing and BOM

PCB LAYOUT

The CLC014 requires proper high-speed layout techniques to obtain best results. A few recommended layout rules to follow for best results when using the CLC014 Adaptive Cable Equalizer are:

1. Use a ground plane.
2. Decouple power pins with 0.01 µF capacitors placed ≤ 0.1” (3mm) from the power pins.
3. Design transmission lines to the inputs and outputs.
4. Route outputs away from inputs.
5. Remove ground plane ≥ 0.025” (0.06mm) from the input and output pads.

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REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	19

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